ABSTRACT

In this paper a new technique is introduced that allows for the variable step-size simulation of wave digital filters. The technique is based on the preservation of the underlying network variables which prevents fluctuation in the stored energy in reactive network elements when the step-size is changed. This method allows for the step-size variation of wave digital filters discretized with any passive discretization technique and works with both linear and nonlinear reference circuits. The usefulness of the technique with regards to audio circuit simulation is demonstrated via the case study of a relaxation oscillator where it is shown how the variable step-size technique can be used to mitigate frequency error that would otherwise occur with a fixed step-size simulation. Additionally, an example of how aliasing suppression techniques can be combined with physical modeling is given with an example of the polyBLEP antialiasing technique being applied to the output voltage signal of the relaxation oscillator.

1. INTRODUCTION

The physical modeling of analog reference systems is typically done using three main paradigms: wave digital filters (WDFs) [1][5], state space filters [6][8] and port-Hamiltonian [9] modeling. The WDF technique was developed in the 1970s with the digitization of classical ladder/lattice filters in mind. A need to retain the passivity of the original reference circuits was required so that the simulations would be stable under finite numeric conditions.

Since the early days of WDFs, the theory has evolved considerably in part due to interest from the physical modeling community in modeling historic audio circuits. The interest from this community has led to the development of new techniques that allow for the simulation of circuits containing complex topologies [4][10][11] and multiple/multiport nonlinearities [3][12][13]. There are also many interesting case studies of the simulation of reference circuits containing nonlinear network elements including distortion circuits containing diodes [14][15], tube amplifiers containing triodes [17][20] and circuits containing operational amplifiers (op amps) [14][21].

The digital synthesis of classic analog waveforms and the antialiasing techniques needed to reduce their aliasing in the digital domain is another important thread of research. While there are a large number of techniques for synthesizing these signals, one of the main methods involves bandlimiting the analog versions of the waveforms (or their derivatives) and either directly sampling the bandlimited version or forming approximate correction functions from it using polynomial interpolation [22][23]. A variant of the latter technique has also been applied to antialiasing in nonlinear waveshaping [25][26]. Recently, a new antialiasing technique has been introduced in [26] and expanded upon in [27] that is based upon the differentiation of the antiderivatives of memoryless nonlinearities. The idea of combining physical modeling and antialiasing techniques has been suggested in [27].

To motivate the use of the variable step-size simulation method as well as provide an example of how physical modeling and antialiasing techniques can be combined, we study a square wave oscillator circuit commonly known as a relaxation oscillator. This circuit comes from a larger class of more complex oscillator circuits and was chosen to study due to its simplicity as well as two challenges that its simulation presents: significant frequency error which occurs when running the simulation with a fixed step-size and the need for an antialiasing method to suppress the aliasing present in the output waveform.

These two challenges are addressed as follows. First, the frequency error is reduced using the new variable step-size WDF simulation technique. Secondly, antialiasing of the output waveform is accomplished using the polyBLEP method [24], where domain knowledge of the circuit is used to estimate the exact location of the discontinuities in the output waveform.

In Section 2 a previous variable step-size WDF technique is reviewed and the new method is presented. The case study of the relaxation oscillator is given in Section 3. The circuit and its components are described in detail in Section 3.1. Section 3.2 explains how the WDF model of the circuit is derived and, in particular, how the op amp is implemented. The issues encountered when running the simulation with a fixed step-size are detailed in Section 3.3 and the way in which the new variable step-size technique is used to counter them is presented in Section 3.4. The technique in which polyBLEP is used to suppress output signal aliasing appears in Section 3.6 which is followed by the concluding thoughts in Section 4.

2. VARIABLE STEP-SIZE SIMULATION

Historically, WDFs were formulated to run at a fixed step-size using voltage waves [1] which are defined:

\[
\begin{align*}
    a &= \frac{1}{2}(v + i) \\
    b &= \frac{1}{2R}(v - i)
\end{align*}
\]

where \( a \) is called the “incident” wave, \( b \) is called the “reflected” wave and \( R \) is a free variable called the port resistance which is used to tune the system to eliminate delay free loops. A technique for simulating WDFs with a variable step-size was presented in [28] where it was shown that varying the step-size of an RLC circuit (Figure 1) discretized with the trapezoidal method led to an increase in energy in a zero-input simulation when it should have been passive. Their solution to the problem was to run the
variable step-size simulation on an equivalent circuit where the inductor was replaced with a network equivalent gyrator and capacitor pair. They stated that the equivalent circuit corresponded to discretization using the Gauss (midpoint) method and demonstrated that it exhibited the expected behavior of the reference circuit. Since their method depends on the replacement of inductors with network equivalent devices it is unclear whether the method will be guaranteed to work for all possible reference circuits.

In this section we introduce a new technique which allows WDFs discretized with any passive discretization technique, in particular the trapezoidal method, to be simulated with variable step-sizes. The development of the new technique was motivated by the fact that it was not obvious how the technique from [28] can be used with the relaxation oscillator circuit presented in the case study in Section 3.1. In Section 2.1 the general technique will be introduced and described. Later, in Section 3.4 it will be shown how varying the step-size fails to work with the example circuit and how the new technique can be used to mitigate the encountered issues.

2.1. Variable Step-Size WDF Simulation Technique

The variation of step-size in a WDF discretized with the trapezoidal rule (or other passive discretization technique) requires careful consideration due to the intricate relationship between the sampling rate and reactive network elements. Looking at the definition of wave variables (Equation (1)) and the port resistance values for reactive elements (Table 1) it is clear that the wave variables of these elements are directly coupled to the sampling rate.

The stored energy of a passive network is given by [28]:

$$E_k = \frac{1}{2} \sum \left[ R_k \left( a_k^2 + b_k^2 \right) + L_k \left( a_k^2 - b_k^2 \right) \right]$$

where $a_k$ and $b_k$ are the wave variables (Equation (1)), and $R_k$ and $L_k$ are the port resistances and port inductances, respectively.

Following the definition of wave variables, we define the new wave variables in terms of voltage, current and port resistance by:

$$\begin{align*}
\hat{a} &= v + R_{k+1} i \\
\hat{b} &= \frac{v - R_{k+1} i}{2R_k}
\end{align*}$$

We then define the new wave quantities in terms of voltage, current and the new port resistance by:

$$\begin{align*}
\hat{a} &= v + R_{k+1} i \\
\hat{b} &= \frac{v - R_{k+1} i}{2R_k}
\end{align*}$$

Combining these two sets of equations in matrix form yields the following conversion matrix:

$$\begin{pmatrix}
\hat{a} \\
\hat{b}
\end{pmatrix} = \frac{1}{2R_k} \begin{pmatrix}
R_k + R_{k+1} & R_k - R_{k+1} \\
R_k - R_{k+1} & R_k + R_{k+1}
\end{pmatrix} \begin{pmatrix}
a \\
b
\end{pmatrix}$$

In practice, however, $b$ does not get used as the reflected waves of both inducers and capacitors only depend on $\hat{a}$. Through this transformation, both the power and the energy stored in the unit delays is preserved across step-sizes.

As a demonstration of the validity of this method, it was ran on the example RLC circuit used in [28] (Figure 1). The inductor incident waves from the simulation are shown in Figure 2 computed without correcting the wave quantities (as shown in the original paper), computed with our technique and also computed with a fixed step-size. As seen in the fixed step-size simulation trace, the traces should be exponentially decaying sinusoids. This correct behavior is seen in the trace of the simulation using the proposed technique. The trace is exponentially growing, however, when the wave quantities are not corrected.

To reiterate the process of correcting the wave variables, the following steps must be taken any time the sampling rate is altered:

1. Store the wave variables for all reactive elements and elements that appear above them in shared subtrees.
2. Readapt those network elements with the port resistance corresponding to the new sampling rate.
3. Convert the stored wave variables using the conversion matrix of Equation (3).
4. Update the relevant network elements with the converted wave variables.
5. If the structure contains an $R$-type adaptor, update $S$, $H$, $E$, $F$, $M$ and $N$ using the updated port resistance values.
6. If wave quantities need to be output, convert them to a single unified representation (such as the one relating to audio rate).
3. RELAXATION OSCILLATOR CIRCUIT CASE STUDY

3.1. Circuit Description

The circuit to be modeled is called a relaxation oscillator [30] and is also known as an astable multivibrator circuit [31]. It contains the following components: a resistor \( R_1 \), a capacitor \( C_1 \), a voltage divider (\( R_2 \) and \( R_3 \)) and an op amp. Throughout this paper it is assumed that \( R_2 = R_3 \) and that the op amp operates from rail-to-rail. The circuit schematic is shown in Figure 3.

![Relaxation Oscillator Schematic](image)

Figure 3: Relaxation Oscillator Schematic.

The basic operation of the circuit is to behave as a comparator whose output swings high or low based on the whether the input voltage to the op amp is above or below a certain threshold value.

![Traces of the op amp input voltage, op amp output voltage and the capacitor voltage](image)

Figure 4: Traces of the op amp input voltage, op amp output voltage and the capacitor voltage.

The component values used during all simulations are given in Table 2. The capacitor value was used to control the frequency of oscillation and thus set based on the desired simulation frequency \( F_0 \) per Equation (4).

### Table 2: Relaxation Oscillator Circuit Component Values

<table>
<thead>
<tr>
<th></th>
<th>( R_1 )</th>
<th>( R_2 )</th>
<th>( R_3 )</th>
<th>( C_1 )</th>
<th>( V_{\text{max}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Omega )</td>
<td>10 k</td>
<td>10 k</td>
<td>10 k</td>
<td>1/((2 \log(3)/R_1C_1))</td>
<td>9 V</td>
</tr>
</tbody>
</table>

The comparator is configured as a Schmitt trigger by means of the positive feedback path between \( v_{\text{out}} \) and \( i_{\text{in}} \). Assuming that the op amp is powered with a rail voltage of \( \pm V_{\text{max}} \) and that it begins with the op amp in positive saturation, the capacitor begins charging towards \( +V_{\text{max}} \) with the time constant defined by \( R_1C_1 \). When the capacitor reaches \( V_{\text{max}}/2 \), the op amp flips over to negative saturation and the capacitor begins discharging towards \( -V_{\text{max}} \). This behavior is illustrated in Figure 4 starting at sample number 50.

The period and frequency of oscillation are given by the following equations [31]

\[
\begin{cases}
T_0 = 2 \log(3) R_1 C_1 \\
F_0 = 1/T_0
\end{cases}
\]  

(4)

The component values used during all simulations are given in Table 2. The capacitor value was used to control the frequency of oscillation and thus set based on the desired simulation frequency \( F_0 \) per Equation (4).

3.1.1. Op Amp Modeling

Operational amplifiers are very important devices in audio circuit design. Since, on the component level, op amps are composed of many passive electrical devices and potentially dozens of transistors, they are often modeled during design and simulation using simplified models. Depending on the level of detail needed, various techniques can be used to model op amps. More complicated linear “macromodels” are built up using linear one-ports (resistors, capacitors and dc sources) and two-ports (controlled sources) and can account for many observed op amp behaviors. In the virtual analog context these models may be too complex when only one particular aspect of the model is needed. In the context of the relaxation oscillator the op amp behaves as a comparator. Based on the difference in voltage between the positive and negative terminals of \( v_{\text{in}} \), the op amp output goes into either positive or negative saturation.

A comparator may be represented ideally as a two-port nonlinear voltage-controlled voltage source (VCVS). This two-port device enforces two network constraints. The first is the nonlinear function \( v_{\text{out}} = V_{\text{max}} \text{sgn}(v_{\text{in}}) \) and the second is the no input current criterion \( i_{\text{in}} = 0 \). We call \( v_{\text{out}} \), \( i_{\text{in}} \) the dependent variables and \( v_{\text{in}}, i_{\text{out}} \) the independent variables and let

\[
x_C = [v_{\text{in}} \ i_{\text{out}}]^T \quad \text{and} \quad y_C = [i_{\text{in}} \ v_{\text{out}}]^T.
\]  

(5)

From this we define the nonlinear relationship as

\[
y_C = f(x_C) = \begin{bmatrix} 0 \\ V_{\text{max}} \text{sgn}(v_{\text{in}}) \end{bmatrix}.
\]  

(6)

This particular comparator model was chosen to enforce an instantaneous transition between \( \pm V_{\text{max}} \) which exactly matches the step discontinuity which the polyBLEP method is designed to work with (see Section 3.6).
3.2. WDF Model of the Circuit

We form the WDF model using the techniques from [3,4]. Either by visual inspection or via graph theoretic techniques, the schematic is rearranged as in Figure 5a so that all series and parallel subtre es are separated from the two-port nonlinearity by the remaining complex connections which are collectively called the $\mathcal{R}$-type adapter.

The techniques of [3] are used to determine the scattering behavior of the $\mathcal{R}$-type adapter which is represented by the matrix $S$. The following system of equations fully describes the relationship between the $\mathcal{R}$-type adapter and the two-port nonlinearity:

\[
\begin{align*}
\begin{bmatrix}
y_C \\
x_C \\
b_E \\
E \\
F \\
M
\end{bmatrix} &= \begin{bmatrix}
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
C_{12} & 0 & 0 & 0 & 0 \\
C_{21} & 0 & 0 & 0 & 0 \\
C_{22} & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
y \\
x \\
v \\
E \\
F \\
M
\end{bmatrix}
\]
\end{align*}
\]  
(7)

where

\[
S = \begin{bmatrix}
S_{11} & S_{12} \\
S_{21} & S_{22}
\end{bmatrix}, \quad H = (I - C_{22}S_{11})^{-1}
\]

and $a_E = [a_3 \ a_4 \ a_5 \ a_6]$ is the vector of incident waves from the $\mathcal{R}$-type adapter.

\[\text{(a) Schematic Rearranged.} \quad \text{(b) WDF.}\]

Figure 5: Relaxation Oscillator Rearranged Schematic and WDF.

As discussed in Section 3.1.1 the input variables, output variables and comparator model of the op amp are given by Equations (5) and (6). We then use the definition of voltage waves (Equation (1)) and the signal flow relationship of the nonlinear device quantities:

\[
\begin{bmatrix}
x_C \\
b
\end{bmatrix} = C
\begin{bmatrix}
y_C \\
a
\end{bmatrix}
\]

where

\[
b = \begin{bmatrix}
b_1 \\
b_2
\end{bmatrix} \quad \text{and} \quad a = \begin{bmatrix}
a_1 \\
a_2
\end{bmatrix},
\]

to determine the generalized conversion matrix $C$ [29]:

\[
C = \begin{bmatrix}
C_{11} & C_{12} \\
C_{21} & C_{22}
\end{bmatrix}
\]

where $R_1$ and $G_2$ refer to the port resistance and port conductance of ports 1 and 2, respectively.

3.3. Problems Resulting from the Fixed Step-size Simulation

3.3.1. Simulation Error

By running the simulation with a fixed step-size at a variety of frequencies and then analyzing the spectrum of the output voltage of the op amp it was determined that a noticeable amount of frequency error was occurring in the simulation. Upon more detailed analysis of the circuit output, it was determined that the majority of the error was occurring around the location of the discontinuities in the component voltages.

As shown in Figure 5b there are two related error scenarios. In the first, as seen in Figure 5ba it is possible that the error leads to the simulation running at a lower frequency than desired due to an overshoot at the first transition of the capacitor voltage. In the second scenario, Figure 5bb the opposite situation occurs and however, the nonlinear relationship is modeled as a step discontinuity for which iterative techniques struggle to converge quickly if at all. Through inspection of the WDF equations representing the nonlinearity it was found that they are formed in such a way that a quasi-analytic solution can be determined.

From Equation (6), we get the following complete description of the nonlinear system of equations to be solved:

\[
x_C = Ea_E + Fy_C
\]

where, for this particular circuit, $E$ is a $2 \times 4$ matrix and $F$ is a $2 \times 2$ matrix. We use domain knowledge of the circuit to simplify the nonlinear system of equations. Since $a_3$, $a_4$ and $a_6$ are the incident waves relating to the resistors, which are always zero, and since $i_{in}$ is also zero, the following simplified expression is obtained:

\[
\begin{bmatrix}
v_{in} \\
v_{out}
\end{bmatrix} = \begin{bmatrix}
\epsilon_{13}a_5 + f_{12}V_{max} \text{sgn}(v_{in}) \\
\epsilon_{23}a_5 + f_{22}V_{max} \text{sgn}(v_{in})
\end{bmatrix}
\]

The values of $v_{out}$ and $i_{out}$ are dependent on the value and sign of $v_{in}$ and the constant values from the $E$ and $F$ matrices. Therefore, the nonlinearity can be solved algorithmically using the following pseudocode:

Algorithm 1: Nonlinearity Solver

1. if $n - 1 < 1$
2. initialize $\text{sgn}_v$ to $\pm 1$
3. else
4. $\text{sgn}_v \leftarrow \text{sgn}(v_{in}(n - 1))$
5. end if
6. $v_{in} \leftarrow \epsilon_{13}a_5 + f_{12}V_{max} \cdot \text{sgn}_v$
7. $x_C \leftarrow Ea_E[n] + F \cdot \begin{bmatrix} 0 & 0 \end{bmatrix}$
8. $\text{sgn}_v \leftarrow -\text{sgn}_v$
9. $v_{in} \leftarrow \epsilon_{13}a_5 + f_{12}V_{max} \cdot \text{sgn}_v$
10. $x_C \leftarrow Ea_E[n] + F \cdot \begin{bmatrix} 0 & 0 \end{bmatrix}$
11. return $x_C, y_C$
were observed: the phase-locking of the frequency that occurred from these errors occurred immediately such that the actual simulation frequency error, we derive an expression for the worst case error in order to investigate the general behavior of the worst case error curves in cents can be derived using the following formula:

\[ F_{\text{max}} = 1200 \max \left( \left\lceil \log_2 \left( \frac{F_0}{F_s} \right) \right\rceil, \left\lfloor \log_2 \left( \frac{F_s}{F_0} \right) \right\rfloor \right) \]  

where \( F_s \) is the sampling rate. Equation (10) gives the worst case frequency error estimation as determined by the largest possible rounding error occurring in the simulation period.

A portion of the resulting curve is shown in Figure 7a. The minimum points on the curve corresponding to an error of one sample occur at odd integer periods which are equal distance from the nearest even integer periods. From those points, the error curve increases in either direction approaching a theoretical limit of two samples (indicated by open circles). Finally, at the even integer period values, there is no error in the period which is notated by the solid black dots. The dotted red line shows the maximum error limit which was used in the computation of the frequency error curves shown in Figure 7b.

Hypothetically assuming that a frequency error of six cents is imperceptible at all frequencies, the worst case error curves (Figure 7b) given an idea of the level of oversampling necessary for the fixed step-size simulation error to fall below that level. It is also evident that the maximum possible simulation error is frequency dependent and clearly increasing with frequency. Thus, the amount of oversampling necessary to mitigate the worst case error is coupled to the desired frequency of simulation.

3.4. Variable Step-size Simulation of the Oscillator WDF

Variable step-size ODE solvers typically utilize an automatic step-size selection algorithm \cite{28, 32}. The step-size is determined by estimating the amount of simulation error that would result from continuing to use the current step-size and then either increasing or decreasing the step-size based on the result of that error calculation.

Since the majority of the simulation error in the fixed step-size simulation of the relaxation oscillator occurs in the region of the discontinuities in the simulation voltages and the accuracy of the simulation frequency is coupled to the amount of oversampling performed, it would be highly desirable to limit oversampling to just those regions and to also have control over the rate of oversampling. This would have the benefit of reducing the computational cost as compared to just oversampling the simulation with a

Figure 6: Capacitor voltage error scenarios.
3.4.2. Extrapolation and Variable Step-size Algorithm

Algorithm 2 gives pseudocode for the extrapolation and step-size modification routine used in the simulation. The algorithm detects if a zero-crossing will happen in the op amp input voltage during the next two future samples. If so, the system is updated to the higher sampling rate and runs the equivalent of three original rate samples at the higher rate. Only the higher rate samples corresponding to lower rate samples are stored (with wave quantities converted to the lower rate representation) so that the output of the simulation always corresponds to the base sampling rate. Finally, the system returns to running at the original sampling rate until the next discontinuity is detected. It is enforced that the higher sampling rate is an integer multiple of the base sampling rate so that interpolation can be avoided during decimation.

Algorithm 2: Extrapolation/Step-Size Algorithm

\[
\begin{align*}
\text{extrapolate } & v_{in}[n] \text{ from } v_{in,n} \text{ using Equation (11)} \\
\text{extrapolate } & v_{in,p} \text{ from } v_{in,n} \text{ using Equation (11)} \\
\text{if } & v_{in,n} - v_{in,p} \leq 0: \\
& nSamps = 3 \\
& K = \text{the oversampling factor} \\
& k = nSamps \cdot K \\
& \text{Update system to new sampling rate} \\
& \text{for } i = 1: k \\
& \text{iterate system 1 sample} \\
& \text{if } i \mod K = 0 \\
& \text{save system values as } (n+i/K-1)-\text{th values} \\
& \text{convert saved wave quantities using Eq. (3)} \\
& \text{end if} \\
& \text{Update system back to original sampling rate} \\
& \text{end if}
\end{align*}
\]

It should be noted that anti-aliasing is not performed at the decimation stage. This is because the anti-alias filtering of \( v_{in} \) will change the dynamics of the system, through modification of the output voltage, affecting the energy stored in the capacitor therefore affecting the frequency of oscillation. In order for the simulation frequency to be as accurate as possible, which corresponds to the simulation error being as small as possible, we allow the aliasing to occur within the simulation. How to suppress the aliasing inherent in the output voltage is the subject of Section 3.6.

3.5. Variable Step-size Method with the Relaxation Oscillator Simulation

In Section 2 a new technique was introduced for the variable step-size simulation of a WDF. The need for the technique arose from the fact that the relaxation oscillator is a nonlinear circuit and also does not contain any inductors. Therefore, it was unclear how the technique from [28] could be implemented with this particular circuit. If the Gauss method is equivalent to the trapezoidal rule for any circuit that does not contain any inductors. Therefore, it was unclear how the technique from [28] could be implemented with this particular circuit. If the Gauss method is equivalent to the trapezoidal rule for any circuit that does not contain any inductors, then variable step-size simulation without using the technique presented in Section 2 will lead to large fluctuations in the energy stored in the delay registers of the capacitor.

This can be clearly seen in Figure 8 which shows the incident waves and stored energy of the capacitor from three different simulations. The desired fundamental period of the simulation was 100.25 samples so that a fixed step-size simulation run at 8 × oversampling would yield an output waveform with no frequency error. The corrected and uncorrected traces show the incident waves of the capacitor when trapezoidal discretization is used with and without the technique proposed in Section 2. The figure shows that large fluctuations in stored energy occur when the step-size
In the original method, the square wave is generated using a
phase accumulator which allows for an exact calculation of the
location of the discontinuities. This fractional delay value is then
used to determine the exact placement of samples of the polyBLEP
residual function which are added to one or more samples of the
output waveform before and after each discontinuity.

The WDF simulation of the example circuit in this paper does not
lend itself to a simple determination of the phase of the op
amp output voltage. We use a method based on the extrapolation
technique developed in Section 3.4.1 for determining the fractional
delay of the occurrence of each discontinuity. During the higher
rate processing, after the polarity of the input voltage has flipped,
a version of Equation (11) is used to determine the fractional
delay in terms of the higher sampling rate:

\[ dx_K = 1 + R_1 C_1 K F_s \log \left( \frac{\text{sgn}(v_{in}[i-1]) V_{\text{max}}}{\text{sgn}(v_{in}[i-1]) V_{\text{max}} + 2 v_{in}[i-1]} \right). \]

From this, the fractional delay is expressed in terms of the
original sampling rate by adding the distance to the next lower rate sample:

\[ d = \frac{(K - i) \mod K}{K} \]

to the appropriately scaled fractional delay value:

\[ dx = \frac{dx_K}{K} + d \]

where \( i \) and \( K \) are as defined in Algorithm 2.

Depending on the chosen polyBLEP method, a number of \( v_{out} \)
samples before and after the step discontinuity have to be altered
to include the polyBLEP residual amount for the chosen scheme.
This is done exactly the same way as in the original paper.

Due to the effect that the polyBLEP residual has on the dynamics
of the simulations, the polyBLEP residual is applied to a
separate output signal path so that it does not affect the internal
dynamics of the simulation. Thus, the modified output voltage is
not fed back through the feedback path of the circuit.

Third-order Lagrange polynomial polyBLEP residual functions
were used to reduce the aliasing for a simulation run with a funda-
mental frequency of 100 Hz at a sampling rate of 44.1 kHz with
a higher rate of 16 × \( F_s \) for a frequency error of 9.7e−4 cents.
The result of applying the polyBLEP residual function to the output
voltage is shown in Figure 9 where the upper image shows the spectrum of
the original output voltage and the lower image shows the spectrum of
the output voltage with the polyBLEP residual applied. Clearly, the aliasing in the spectrum of the output voltage
with polyBLEP residuals applied is falling off at a much steeper
rate than the original waveform’s spectrum. It is also evident that
the amplitude of the higher harmonics in the spectrum of the alias
suppressed waveform are falling off more quickly than the theoretical
amplitudes. This can be fixed using a high shelf equalization
filter. Example filter coefficients are given in [24].

3.6. Aliasing Suppression in the Output Signal

Due to the use of the ideal comparator VCVS characteristic to
model the op amp behavior, the output voltage of the op amp is a
square wave that instantaneously switches between \( \pm V_{\text{max}} \). Thus, the
presence of step discontinuities in the output waveform results
in a similar amount of aliasing as arises from trivial synthesis of
a square waveform. To minimize the aliasing, we use the poly-
BLEP [23] antialiasing technique.

In the original method, the square wave is generated using a
phase accumulator which allows for an exact calculation of the
location of the discontinuities. This fractional delay value is then
used to determine the exact placement of samples of the polyBLEP
residual function which are added to one or more samples of the
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\[ dx_K = 1 + R_1 C_1 K F_s \log \left( \frac{\text{sgn}(v_{in}[i-1]) V_{\text{max}}}{\text{sgn}(v_{in}[i-1]) V_{\text{max}} + 2 v_{in}[i-1]} \right). \]

From this, the fractional delay is expressed in terms of the
original sampling rate by adding the distance to the next lower rate sample:

\[ d = \frac{(K - i) \mod K}{K} \]

to the appropriately scaled fractional delay value:

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where \( i \) and \( K \) are as defined in Algorithm 2.

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samples before and after the step discontinuity have to be altered
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This is done exactly the same way as in the original paper.

Due to the effect that the polyBLEP residual has on the dynamics
of the simulations, the polyBLEP residual is applied to a
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dynamics of the simulation. Thus, the modified output voltage is
not fed back through the feedback path of the circuit.

Third-order Lagrange polynomial polyBLEP residual functions
were used to reduce the aliasing for a simulation run with a funda-
mental frequency of 100 Hz at a sampling rate of 44.1 kHz with
a higher rate of 16 × \( F_s \) for a frequency error of 9.7e−4 cents.
The result of applying the polyBLEP residual function to the output
voltage is shown in Figure 9 where the upper image shows the spectrum of
the original output voltage and the lower image shows the spectrum of
the output voltage with the polyBLEP residual applied. Clearly, the aliasing in the spectrum of the output voltage
with polyBLEP residuals applied is falling off at a much steeper
rate than the original waveform’s spectrum. It is also evident that
the amplitude of the higher harmonics in the spectrum of the alias
suppressed waveform are falling off more quickly than the theoretical
amplitudes. This can be fixed using a high shelf equalization
filter. Example filter coefficients are given in [24].

4. CONCLUSION

In this paper a new technique was introduced for the variable step-
size simulation of wave digital filters. A conversion of the wave
variable quantities of reactive network elements is performed any
time that the sampling rate is changed. Our method is novel in that
it ensures that the network variables are preserved which enforces
that the energy stored in the reactive elements is preserved as well.
In [28], the variable step-size simulation of WDFs discretized with the trapezoidal rule was identified as an open problem. By identifying the relationship between wave variables and network variables it has been shown how the correct behavior can achieved in a WDF model which directly discretizes the reactive elements and does not use network component equivalencies. The validity of the technique holds regardless of the discretization technique being used to discretize the reactive network elements. With WDFs, however, it is well known that passive discretization techniques must be used.

Through the case study of a relaxation oscillator circuit, the need for the new variable step-size technique was demonstrated. The variable step-size WDF simulation technique was used to mitigate frequency error related to the discontinuities in the device voltages. An extrapolation formula was used to estimate the occurrence of future zero crossings in the input voltage of the op amp. This allowed the system to be switched to the higher simulation rate for a short duration of three base rate samples encompassing the occurrence of the step discontinuity in the op amp output voltage. It was also demonstrated how physical modeling and antialiasing techniques can be combined to yield an accurate and alias-reduced simulation of the relaxation oscillator circuit. The polyBLEP antialiasing technique was used and the oversampling from the variable step-size technique had the additional benefit of improving the estimate of the fractional delay thus further improving the accuracy of the polyBLEP method.

5. REFERENCES